In the specification:

Please replace paragraph number 008, at page 3, with the following paragraph:

Another aspect of the invention concerns ~~of~~ programming PLDs. In one illustrative embodiment, a method for configuring a PLD includes receiving serial configuration data. The serial configuration data are adapted to configure a function of the PLD. The method also includes configuring the function of the PLD by using the serial configuration data. The PLD is configured without buffering the serial configuration data.

Please replace paragraph number 0019, at page 5, with the following paragraph:

This invention contemplates apparatus and associated methods for configuring programmable electronic circuitry, such as PLDs. Conventionally, PLD configuration suffers from stalling of the configuration device or the slowing down of the configuration process because the control circuitry of the PLD cannot decompress the configuration data and program or configure the PLD simultaneously.

Please replace paragraph number 0026, at page 7, with the following paragraph:

FIG. 1 shows a general block diagram of a PLD 103 according to an illustrative embodiment of the invention. PLD 103 includes configuration circuitry 118, programmable logic circuitry 115, and programmable interconnect circuitry 112. Additionally, and as desired, PLD 103 may include one or more data processing blocks or hardware 114, such processor, communications circuitry, memory controllers, and the like, as persons of ordinary skill in the art who have the benefit of the description of the invention understand.

Please replace paragraph number 0035, at page 10, with the following paragraph:

CRAM 138 uses the processed configuration data to configure the functionality of PLD 103, as persons of ordinary skill in the art who have the benefit of the description of the invention understand. Thus, CRAM 138 may configure the functionality of the

programmable or configurable resources of PLD 103, such as programmable logic circuitry 115 and programmable interconnect circuitry 112.

Please replace paragraph number 0058, at page 16, with the following paragraph:

The last data word in FIG. 6 has a binary value 0001100001011010, which results in data nibbles 0001 1000 0101 1010, header bits 1, 1, 1, and 1, and control nibble 1111. Control nibble 1111 and the original data bits form the representation of the data word. Note ~~this~~ that, in this situation, where each data nibble includes a binary one digit, the representation of the data word does not result in any compression.

Please replace paragraph number 0072, at pages 20-21, with the following paragraph:

Decompression state machine ~~203~~ 209 uses enable (*EN*) signals 212A-212D to enable and control the loading of data into data registers 215A-215D, respectively. More specifically, each of data registers 215A-215D receives serial data signal 224. Decompression state machine ~~203~~ 209 uses enable signals 212A-212D to control which of data registers 215A-215D loads serial data 224 on the next occurrence of clock signal 221.

Please replace paragraph number 0081, at page 23, with the following paragraph:

Note that it takes four clock cycles for four control nibbles to load. Note further that, on the third clock cycle, decompression state machine 209 clears data registers 215A-215D. Because of this sequence of events, decompression state machine ~~203~~ 209 has enough time to provide two bytes of data as parallel configuration data 233 before the next four control nibbles load. In this manner, embodiment 200 avoids stalling the configuration device or slowing down the configuration process without using a buffer.

Please replace paragraph number 0082, at page 23, with the following paragraph:

If serial data 224 has an uncompressed format, the data converter operates as follows. The data converter receives serial data 224 in response to clock signal 221.

Decompression state machine ~~203~~ 209 causes data registers 215A-215D to load four nibbles (*i.e.*, 16 bits) of data extracted from the serial data.

Please replace paragraph number 0083, at page 24, with the following paragraph:

Decompression state machine ~~203~~ 209 also causes data registers 215A-215D and MUX 230 to provide two bytes of configuration data as parallel configuration data 233. Other parts of PLD 103 may subsequently use the parallel configuration data to program various blocks and circuitry within PLD 103, as described above. Note that, in this mode of operation, other circuitry and signals in the data converter operate as described above.